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Please replace the paragraph beginning on page 21, line 6, with the following rewritten paragraph:

In some cases, the circuitry used to alter current applications along the bit and/or digit lines of MRAM device 10 may be used to identify "errant" magnetic elements. In particular, during the course of altering current along the bit and/or digit lines of the device, errant magnetic elements, such as selected cells which ~~are~~ require too large of a current to switch their magnetization or disturbed cells which change their magnetization at a low current level, may be detected. Such errant magnetic elements may be discarded and, in some embodiments, replaced, improving the reliability of the device. In general, the circuitry used to alter current applications of current to magnetic memory arrays 12 to identify errant elements, create a probability switching distribution and/or determine an optimum programming current may include any one or combination of circuitry included in adjustable pulse delay 16, adjustable pulse width 20, program pulse timing generator 18, north bit line pulse generator 22, south bit line pulse generator 58, digit line pulse generator 56 and/or adjustable pulse amplitudes 24, which are discussed in more detail below.

Please replace the paragraph beginning on page 25, line 24, with the following rewritten paragraph:

An exemplary configuration for adjustable bias voltage 30 is illustrated in Fig. 8. As shown in Fig. 8, adjustable bias voltage 30 may include transistors 100 and 102 and DAC 106 including resistor 108. Reference voltage V_{ref} may be applied to line 110 passing through resistor 108 to generate bias reference voltage VBIASREF along line 112. The settings of DAC 106 may be used to alter the resistance of resistor 108 and, therefore, may be used to alter bias reference voltage VBIASREF. In general, the settings of DAC 106 may be controlled by data input 82, which may include laser fuses, metal mask options or data transmitted from a magnetic element storage latch arranged within MRAM device 10. Other circuitry other than the one depicted in Fig. 8 may be used to bias voltages applied to magnetic elements of MRAM device 10, depending on the design characteristics of the device. As such, the adjustable bias voltage circuit provided herein is not necessarily restricted to the circuitry illustrated and described in reference to Fig. 8. In other embodiments, the bias voltage circuit provided herein may be omitted from MRAM device 10. In particular, the inclusion of such circuitry is not necessarily needed for the operation of MRAM device 10.